1. An ESD protection device with complementary dual drain implant comprising:

a) an N-well implanted in a P-substrate;

b) an N+ diffusion implanted on top of said N-well, such that said N+ diffusion extends into said P-substrate on both sides of said N-well;

c) where said N+ diffusion is shared by the drains of two adjacent NMOS transistors;

d) a pad coupled conductively to said N+ diffusion between said drains; and

e) a P-ESD implant interposed between said N+ diffusion and said N-well such that said N-well is electrically coupled to said N+ diffusion, where said P-ESD implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage of the drain/P-substrate junction.

2. The ESD protection device of claim 1, wherein the implant dosage for said P-ESD implant is less than the implant dosage for said N+ diffusion but higher than the implant dosage for said N-well.

3. The ESD protection device of claim 1, wherein said P-ESD is electrically coupled to said P-substrate by extending into said P-substrate.

4. The ESD protection device of claim 1, wherein said drains of said two NMOS transistors are at opposite ends of said N-well.

5. The ESD protection device of claim 1, wherein said N-well extends in depth beyond the bottom of said P-ESD implant.

6. An ESD protection device with complementary dual drain implant comprising:

a) an N-well implanted in a P-substrate;

b) an N+ diffusion implanted on top of said N-well, such that said N+ diffusion extends into said P-substrate on both sides of said N-well;

c) where said N+ diffusion is shared by the drains of two adjacent NMOS transistors;

d) a pad coupled conductively to said N+ diffusion between said drains; and

e) a P-ESD implant interposed between said N+ diffusion and said N-well such that said P-ESD implant is embedded within said N+ diffusion and said N-well, where said P-ESD implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage of the drain/P-substrate junction.

7. The ESD protection device of claim 6, wherein sections of said embedded P-ESD implant extend at either end of said P-ESD implant beyond said N-well and said N+ diffusion, said P-ESD implant thus coupling electrically to said P-substrate.

8. The ESD protection device of claim 6, wherein the implant dosage for said P-ESD implant is less than the implant dosage for the N+ diffusion but higher than the implant dosage for said N-well.

9. The ESD protection device of claim 6, wherein said N+ well is electrically coupled to said N+ diffusion.

10. The ESD protection device of claim 6, wherein segments of said P-ESD implant project beyond said N-well, thus extend into said P-substrate when viewed in cross-section.

11. The ESD protection device of claim 10, wherein said segments of said P-ESD implant projecting beyond said N-well maximize the perimeter surface of said P-ESD implant.

12. The ESD protection device of claim 10, wherein said segments of said P-ESD implant projecting beyond said N-well alternate with segments of said P-ESD which are embedded within said N+ diffusion and said N-well.

13. The ESD protection device of claim 6, wherein said N-well extends in depth beyond the bottom of said P-ESD implant.

14. An ESD protection device with complementary dual drain implant comprising:

a) an N-well implanted in a P-substrate;

b) an N+ diffusion implanted on top of said N-well, such that said N+ diffusion extends into said P-substrate on both sides of said N-well;

c) where said N+ diffusion is shared by the drains of two adjacent NMOS transistors;

d) a pad coupled conductively to said N+ diffusion between said drains; and

e) a P-ESD implant interposed between said N+ diffusion and said N-well such that said P-ESD implant is embedded within said N+ diffusion and said N-well, where the P-ESD implant dosage is chosen in such a way as to counterdope said N-well.

15. The ESD protection device of claim 14, wherein said counterdoping creates additional junction areas between said N+ diffusion and said P-ESD implant, where said additional junction areas participate in the avalanche breakdown.

16. The ESD protection device of claim 14, wherein where said P-ESD implant lowers the avalanche voltage of a transistor by reducing the breakdown voltage of the drain- P-substrate junction.

17. The ESD protection device of claim 14, wherein segments of said P-ESD implant, by projecting beyond said N-well, extend into said P-substrate when viewed in cross-section.

18. The ESD protection device of claim 14, wherein said counterdoping creates additional junction areas on those faces of said P-ESD implant which are in contact with said N-well, where said additional junction areas participate in the avalanche breakdown.

19. The ESD protection device of claim 14, wherein electrical connections between said P-ESD implant and said P-substrate are provided in surfaces where said P-ESD implant is in contact with said P-substrate.

20. The ESD protection device of claim 14, wherein said P-ESD implant is interposed between said N+ diffusion and said N-well such that said N-well is electrically coupled to said N+ diffusion.

21. The method of providing ESD protection with complementary dual drain implants, comprising the steps of:

a) creating an N-well in a P-substrate;

b) creating an N+ drain region on top of said N-well, where said N+ drain region projects into said P-substrate on either side of said N-well;

c) creating a P-ESD region between said N+ drain and said N-well, such that said N-well still maintains an electrical connection to said N+ drain region; and

e) providing an implant dosage for said P-ESD implants less than the implant dosage of said N+ drain region but higher than the implant dosage for said N-well.

22. The method of claim 21, wherein said implant dosage for said P-ESD implants is chosen such as to counterdope said N-well underneath said N+ diffusion.

23. The method of claim 21, wherein said P-ESD implant makes electrical contact with said P-substrate.

24. The method of providing ESD protection with complementary dual drain implants, comprising the steps of:

a) creating an N-well in a P-substrate;

b) creating an N+ drain region on top of said N-well, where said N+ drain region projects into said P-substrate on either side of said N-well;

c) creating a P-ESD region between said N+ drain and said N-well, such that first areas of said P-ESD region are surrounded by said N+ drain and N-well; and

e) providing an implant dosage for said P-ESD implants less than the implant dosage of said N+ drain region but higher than the implant dosage for said N-well.

25. The method of claim 24, wherein said implant dosage for said P-ESD implants is chosen such as to counterdope said N-well underneath said N+ diffusion.

26. The method of claim 24, wherein second areas of said P-ESD implant project beyond said N-well into said P-substrate.

27. The method of claim 26, wherein said second areas of said P-ESD implant make electrical contact with said P-substrate.